Attorney Docket No.: BUR920030023US1
Serial No. : 10/605,591

PATENTS

REMARKS

- Claims 1 to 25 are pending
- Claims 1 and 13 are the only independent claims

Claims 1 to 25 stand rejected under 35 U.S.C. Section 102(b) as anticipated by U.S. Patent No. 4,400,771 issued to Suzuki et al. (hereinafter "Suzuki"). Applicants respectfully traverse this rejection.

In rejecting Claims 1 and 13, the Examiner asserts that Suzuki teaches "assigning a fixed ***width*** to one priority of access to memory bandwidth to one or more direct memory access (DMA) machines (53, Fig. 2)" (***emphasis added***). However, Claims 1 and 13 do not recite such a feature. Instead, Claim 1 recites: "assigning a fixed priority of access to memory bandwidth to one or more direct memory access (DMA) machines" and, as amended, Claim 13 recites: "assign[ing] a fixed priority of access to memory bandwidth to the one or more DMA machines." Thus, even if the reference taught that which the Examiner asserts, the reference would not teach the features recited by Applicants. Therefore, Applicants respectfully request withdrawal of the Section 102 rejection for these reasons.

Further, the Examiner supports the above rejection based on reference numeral 53 and Fig. 2 of Suzuki. However, the cited portions to not teach "assign[ing] a fixed priority of access to memory bandwidth to the one or more DMA machines" (or the like) as recited in Applicants' independent claims. Reference numeral 53 in Suzuki is to a directed memory access controller:

> The priority of the direct memory access channel controller 53 is stored in the flip-flops 575 and 576. The contents of the register

> circuit 57, that is to say, the priority information can be changed to set the priority of the processors 51, 52 and 53 in accordance with programs supplied through the processors 51, 52 and 53. For example, processor priority may be programmed as a function of the time of day, or some other predetermined criteria such that processor priority is automatically changed based thereon. (Suzuki, col. 5, lns. 28 to 37)

The text associated with Fig. 2 and reference numeral 53 of Suzuki teach that the priority of the Suzuki DMAC 53 may be set to any desired level and changed based on any desired criteria, for example, time of day. This is clearly distinct from Applicants' system as claimed in which the DMA machines are assigned a fixed priority. The Examiner has not identified, and Applicants cannot find, any teaching within the reference that even suggests assigning fixed priorities to DMA machines. Thus, the reference does not teach this aspect of Applicants' invention and Applicants respectfully request withdrawal of the Section 102 rejection for this additional reason.

Further, Suzuki appears to describe a programmable memory access priority control system for setting priority between multiple processors. In contrast, Applicants' claims are directed to setting priority between a processor and DMA machines serving the processor. Specifically, Applicants' independent Claim 1 recites "priority allocation between . . . one or more DMA machines and the processing unit" and independent Claim 13 recites "allocate[ing] priority of access to the data resource between each of the one or more DMA machines and the processing unit." In addition, Suzuki does not appear to teach or suggest that the "DMA Channel Controller 27" can be assigned a different priority than the processor it serves. In fact, Suzuki does not appear to contemplate the use of one or more DMA machines for each processor. Suzuki appears to only provide a single "DMA Channel Controller 27" for all processors. Thus, the reference does not teach these aspects of Applicants' invention and

Applicants respectfully request withdrawal of the Section 102 rejection for these additional reasons.

Applicants' invention involves a system of DMA/CPU pairs that are controlled and/or coordinated so that all data that must be transferred within specific time constraints is transferred on time. The present invention achieves this by allowing the processor's priority to be adjusted above or below the corresponding DMA machine's fixed priority. In other words, interleaved between the fixed priorities of the DMA machines are priority levels to which the processor may be assigned. In contrast, the Suzuki reference teaches a single DMAC with multiple channels of the same priority. The priority may be changed as described above but the various channels execute transfers in a round robin fashion. Thus the Suzuki system cannot address the problem (*i.e.*, all data that must be transferred within specific time constraints needs to be transferred on time) solved by Applicants' invention.

Applicants believe all pending claims are now in condition for allowance, and respectfully request reconsideration and allowance of the same. Applicants have filed herewith an appropriate Request for Extension of Time. Applicants do not believe any additional Request for Extension of Time is required but if it is, please accept this paragraph as a Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696.

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Serial No. : 10/605,591

PATENTS

Applicants do not believe any other fees are due regarding this amendment. If any other fees are required, however, please charge Deposit Account No. 04-1696. The Applicants encourage the Examiner to telephone Applicants' attorney should any issues remain.

Respectfully Submitted,

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